iSTART

MEMORY TESTING & REPAIRING

iSTART-TEK INC.

芯测科技股份有限公司

iSTART-TEK

is a leading developer in memory testing and repairing solutions and customized design service with innovative and patent protected methodologies, namely configurable architecture.

We offer complete memory testing and repairing solutions on SRAM, Non-Volatile and other types of memories including eFlash, MRAM and RRAM that enable our customers to accelerate design process for better quality and yield.

With the configurable architecture solution featuring low power consumption and high performance, customers can shorten design time effectively while maintaining high quality, establishing irreplaceable leading position in the competitive electronic market.

CORE VALUE

Innovation
We value innovation at every level. We constantly strive to redefine the standard of excellence in everything we do. We want to share our solutions with others so that they might grow into the conventional solutions of tomorrow.

Efficiency
Efficiency is about doing things right. We implement efficient mindset into each aspect, and fulfill into each action . It’ s not about cost cutting — it is about HOW work is done.

Service
Every action we take has our customers in mind. We comply your needs before your request. We pull out all the stops to make the satisfaction of our customers’ paramount.

TECHNOLOGY

Gate-cell Insertion
Designers usually achieve low power design through adding gate cell. START tool provides easy-to-use settings to assist designer to add gate cell and mux in front of MBIST. It avoids manually design problems, also reduces chip developing time.

Multi-Chain Design
Low power design is essential in large scale SoC design. Multi-Chain seperates testing modules into several chains. During testing, power does not supply to the whole chain, but only those tested chains.

Polaris Algorithm
The complexity of Polaris algorithm is 19 times compared to that of MARCH-C, but additional chip area and gate count is only increased by 5%. All memory defects can be detected with such a small amount of area cost.

Programmable Algorithm
Standard testing algorithm like MARCH-C series could not be used in some special memory model. However, with programable algorithm, designers can define their own memory testing method.

User Define Memory
User define memory is a powerful instinct GUI interface. Users can easily input memory modules into EZ-BIST & START tool’ s database and accomplish built-in memory testing circuit by clicks and drags.

Bottom-Up Circuit Insertion

Bottom-up Circuit Insertion enables designers to insert MBIST for those completed modules in advance, avoiding the risk of re-running the process, further shorten the design time.

Repair

Repair function increases yield rate of SoC. START tool supports two repairing mechanisms, namely hard-repair and soft-repair. Besides, START tool also provides stand-alone repairing. Customers can choose repairing mechanisms according to their memory models and design requirements.

Stand-alone Repairing

For those memory models without redundancy, if SoC has memory repairing requirements, START tool's stand-along mechanism can create a stand-alone memory as redundancy. This technology can increase product's yield.

Power-on Self-test

The POT solution allows SoC designers to accomplish power-on self-test design efficiently. POT improves the safety factors of automotive chips. It can also be applied to high reliability electronic devices.

Dynamic Memory Testing

Dynamic memory testing is an unique memory testing technology widely applied in continuous operating system. In SoC design, DMT ensures stability of system and correctness of data.

TECHNOLOGY

EZ-BIST

DESCRIPTION

EZ-BIST features simple setting and easy to use, suitable for developing MCU system which memory instances are less than 50. EZ-BIST is also the best tool for academic and semiconductor research institutions to realize MBIST behavior and implementation. EZ-BIST' s friendly interface and Simplified operation enables users to build BIST circuit instantly, effectively shorten SoC development time, further improves product inspection and reduces development cost.

FEATURE

- Complete GUI interface
- Support UDM (User Defined Memory)
- Support memory grouping setting
- Support auto clock tracing
- Support clicks and drags to memory port insertion
- Support gate-cell insertion for power saving
- Smart error proofing design
- Memory BIST insertion up to 50 instances
- Multiple memory testing algorithms
- Support testing algorithms selection by application & technology node

APPLICATION

- MCU
- IoT
- White Goods
- Medical equipment

TESTING INTERFACE

- JTAG

FIGURE

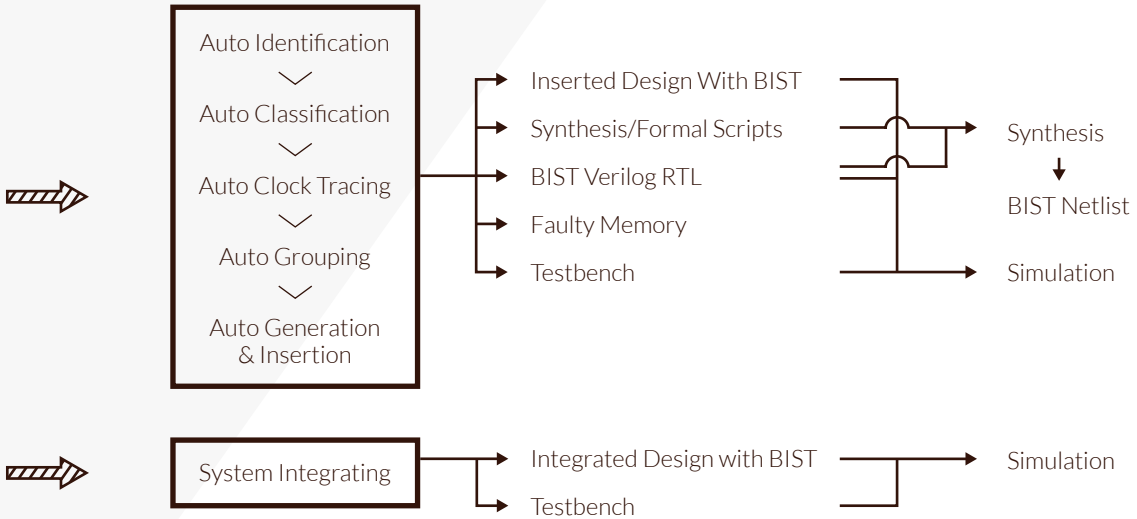
EZ-BIST OPERATION FLOW

BFL (BIST Feature List) Flow

- Insert BIST circuit with memory
- Generate testbench for verifying BIST circuit only

BII (BIST Integration Information) Flow

- Integrate interface of BIST circuit with system top
- Generate testbench for verifying interface of system



START™

DESCRIPTION

START™ v2 (SoC's memory Testing And Repairing Technology) is a complete memory testing and repairing solution for generating BIST and BISR circuit and inserting them into customer's design automatically. START™ v2 's friendly interface and menu style constructive configuration assists users to fulfill DFT for all kinds of IC design simply.

FEATURE

- Support Stand-alone repairing technical for memories without redundancy
- Support UDM (User Defined Memory)
- Support memory grouping setting
- Support auto clock tracing
- Support gate-cell insertion for power saving
- Support POT (Power-On Testing)
- Support DMT (Dynamic Memory Testing)
- Support advanced testing algorithms for MRAM & ReRAM
- Smart fool-proof design
- No Memory instance limitation
- GUI interface
- Advanced repairing architecture
- Multi-chain design
- Bottom-up flow
- Programmable algorithm
- Multiple memory testing algorithms

APPLICATION

- Automotive
- SSD
- Security
- AI
- Edge Computing
- Network
- High Resolution TCON
- AIoT

TESTING INTERFACE

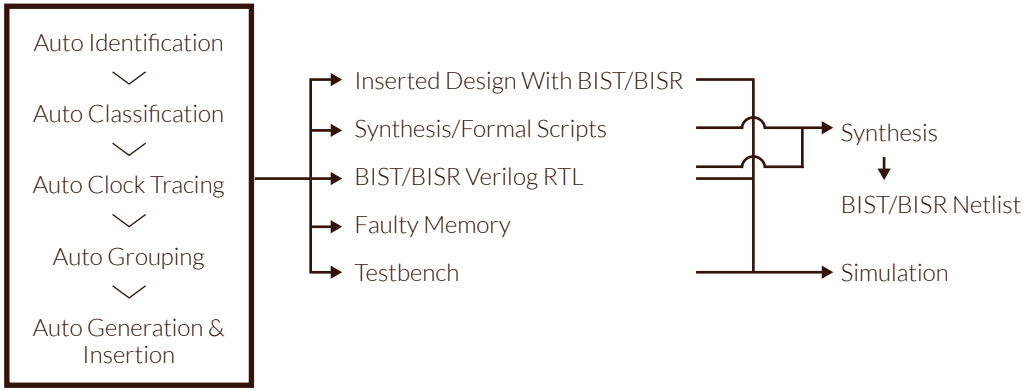
- JTAG
- IEEE 1149.7
- IEEE 1687

FIGURE

START OPERATION FLOW

BFL (BIST Feature List) Flow

- Insert BIST circuit with memory
- Generate testbench for verifying BIST circuit only



BII (BIST Integration Information) Flow

- Integrate interface of BIST circuit with system top
- Generate testbench for verifying interface of system

IP

DESCRIPTION

With accumulated patents and experiences in testing field, iSTART can accomplish MBIST & MBISR according to customers requirements and customize corresponding IPs to customers instantly for all memories, such as eFlash, MTP, SRAM, MRAM ...etc.,. By means of iSTART's unique technology and professional service, customers can significantly improve their product quality and yield rate.

APPLICATION

- eFlash
- MTP
- Particular memory SRAM testing & repairing
- MRAM
- RRAM

TESTING INTERFACE

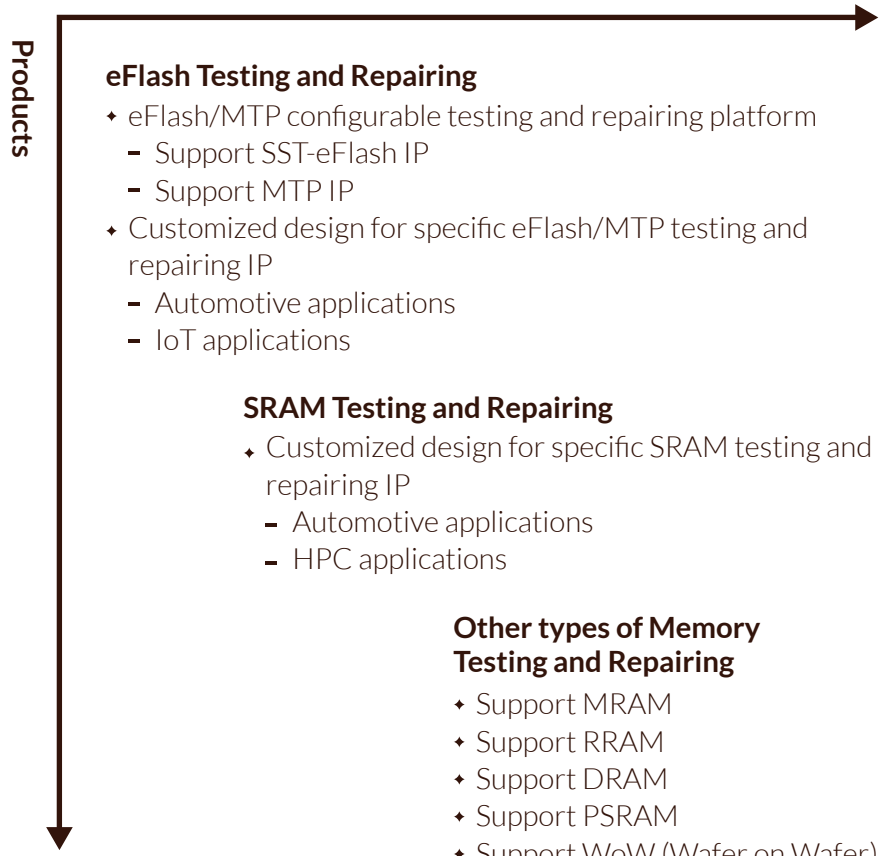
- JTAG
- IEEE 1149.7
- IEEE 1687
- SPI

FEATURE

- Provide testing IPs for all kind of memories
- Support POT (Power-On Test)
- Customized IP testing design
- Support HEART technology (High Efficient Accumulative Repairing Technology)

FIGURE

MAINLINE PRODUCTS OF IP



AI/EDGE COMPUTING

With the development of AI and edge computing, IDC expects that in 2025, 50% of the world's terminal devices will have computer vision and AI neural network computing capabilities. START™ v2 is equipped with bottom-up circuit insertion and polaris algorithm function. Bottom-up circuit insertion enables designers to insert MBIST in advance, effectively lower the risk of re-running. Polaris algorithm is especially suitable for detecting memory defects belonging advanced process.

AUTOMOTIVE

Intelligence, safety and energy saving in automotive industry have driven the vigorous development of automotive electronics. In order to protect passengers' safety, ensuring the reliability of electronic components has been an essential issue. START™ v2 completes Power-on Self-test once power turns on to enhance automotive safety. Clients adopting iSTART solution had passed ISO26262 certification successfully.

SOLUTION

VIDEO/AUDIO

With the increasing advancement of key technologies such as artificial intelligence, deep learning, machine learning, and visual algorithms, image and speech recognition and processing has created various new applications. With programmable algorithm and repair function, designers can select built-in testing algorithm or make customization choices based on their needs; furthermore, START™ v2 can provide diagnosis data and repair memory according to the testing result to increase yield rate.

IOT

It is estimated that by 2025, there will be more than 50 billion connected devices in the world, ranging from smart bracelets, home appliances, to medical equipment. The combination of IoT and AI develops into AIoT, which applications include smart healthcare, smart retail, smart manufacturing and so on. Through iSTART' S friendly GUI interfaces, designers can accomplish memory BIST circuits effectively and maintain as the bellwether in each industry.

iSTART

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